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Scenario-based Run-time Adaptive Multi-Processor System-on-Chip

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Modern embedded systems, which are more and more based on Multi-Processor System-on-Chip (MPSoC) architectures, increasingly require to be adaptive at run time to support complex and dynamic application workloads, dynamic Quality-of-Service management, etc. As one of the approaches for improving the adaptivity of MPSoC systems, dynamic application task (re-)mapping plays a crucial role in exploiting the system properties such that applications can meet their, often diverse, demands on performance and energy efficiency. The research of this thesis aims at improving these dynamic application mapping techniques to increase the efficiency of modern MPSoC systems by adaptively reconfiguring the system according to the dynamic behaviour of application workloads and the status of the target system.

The application task (re-)mapping methods presented in this thesis belong to the class of hybrid task mapping approaches. They overcome the drawback of static task mapping techniques traditionally considered in embedded systems that are unable to support dynamic application behaviour as well as the drawback of pure dynamic (on-the-fly) task mapping techniques that typically only produce mappings of relatively low quality. Our hybrid task mapping approaches have two mapping optimisation stages: design-time static mapping exploration and run-time mapping optimisation/customisation. At design time, two static Genetic-Algorithm based mapping DSE approaches have been proposed to explore partial task mappings (at the level of inter- or intra-application scenarios) for workload scenarios that might appear on the target MPSoC system under optimisation objectives such as performance and/or energy consumption. At run time, a light-weight resource scheduler -- integrated with our proposed mapping optimisation algorithms and a technique for so-called adaptivity throttling -- has been deployed for dynamic system reconfiguration. According to the reason that has triggered the system reconfiguration, the scheduler on the target system is able to dynamically derive near optimal application mappings for the purpose of system reconfiguration based on the mapping information explored at design time. However, applying an adaptivity throttling technique, the actual system reconfiguration will only take place when it has been predicted to be beneficial.

By using our proposed hybrid task mapping techniques, which benefit from both static and dynamic task mapping approaches, the efficiency of MPSoC systems can be considerably improved. On top of this, our techniques also provide solutions for the issues of scalability, flexibility and blind adaptivity that general hybrid task mapping approaches suffer from. Moreover, using a hierarchical control mechanism, we also show that our techniques can perform well on future, large-scale MPSoC systems.